AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1-10 (Canceled)

11. (Withdrawn) A design support apparatus for supporting wiring design for bond wires that connect a semiconductor chip and an interposer, the design support apparatus comprising:

a creating unit that creates simulated design data simulating occurrence of fluctuation in an arrangement position of a semiconductor chip on an interposer and occurrence of fluctuation in bond wire connection terminal positions of the interposer; and

an analyzing unit that analyzes, based on the simulated design data, deficiencies in manufacturing of semiconductor devices due to the fluctuation in the arrangement position of the semiconductor chip on the interposer and the fluctuation in the bond wire connection terminal positions of the interposer.

12. (Withdrawn) A design support apparatus for supporting wiring design for bond wires that connect a semiconductor chip and an interposer, the design support apparatus comprising:

a creating unit that creates simulated design data simulating occurrence of fluctuation in an arrangement position of a semiconductor chip on an interposer and occurrence of fluctuation in bond wire connection terminal positions of the interposer; and

an analyzing unit that analyzes, based on the simulated design data, a tolerance of the fluctuation in the arrangement position of the semiconductor chip on the interposer and a tolerance of the fluctuation in the bond wire connection terminal positions of the interposer.

13. (Currently Amended) A design support apparatus for semiconductor devices comprising:

a first data creating unit that creates, based on design data of a semiconductor package, semiconductor chip simulated arrangement data obtained by arranging a semiconductor chip ~~in a position where fluctuation in an arrangement position of the semiconductor chip in arranging the semiconductor chip on an interposer is simulated;~~ onto the surface of an interposer such that deviation of the semiconductor chip from an original position is simulated;

a second data creating unit that creates, based on the design data of the semiconductor package and the semiconductor chip simulated arrangement data, bond wire simulation data obtained by wiring, using bond wires, the bond wire connection terminals of the semiconductor chip arranged to deviate from an arrangement position in the design data and bond wire connection terminals of the interposer;

a measuring unit that measures a design rule for the bond wires used for the wiring from the bond wire simulation data; and

an analyzing unit that analyzes measurement result obtained by the measuring unit.

14. (Previously Presented) The design support apparatus according to claim 13, wherein the design data of the semiconductor package includes shape of the interposer, shape of the semiconductor chip, an arrangement position of the semiconductor chip on the interposer, shape of the bond wires that connect the semiconductor chip and the interposer, and

arrangement positions of the bond wires that connect the semiconductor chip and the interposer.

15. (Currently Amended) The design support apparatus according to claim 13, wherein the first data creating unit creates semiconductor chip simulated arrangement data obtained by arranging, with respect to the arrangement position of the semiconductor chip on the interposer in the design data of the semiconductor package, the semiconductor chip in a position where ~~fluctuation in~~ deviation of an arrangement position of the semiconductor chip in an in-plane direction or a rotation direction on a semiconductor chip arrangement surface of the interposer or ~~fluctuation~~ deviation in inclination of the semiconductor chip in a thickness direction of the interposer is simulated.

16. (Previously Presented) The design support apparatus according to claim 13, wherein the measuring unit measures clearance between the bond wires and clearance between the bond wires and the semiconductor chip as the design rule.

17. (Currently Amended) The design support apparatus according to claim 16, wherein the analyzing unit analyzes a tolerance of ~~fluctuation in~~ the deviation of an arrangement position of the semiconductor ~~ship~~ chip on the interposer that satisfies the design rule.

18. (Currently Amended) The design support apparatus according to claim 16, wherein the analyzing unit analyzes a tolerance of ~~fluctuation in~~ the deviation of the bond wire connection terminal positions of the interposer that satisfies the design rule.

19. (Previously Presented) The design support apparatus according to claim 13, comprising

a storing unit that stores therein the measurement result.

20. (Previously Presented) The design support apparatus according to claim 13, comprising a storing unit that stores therein analysis result obtained by the analyzing unit.